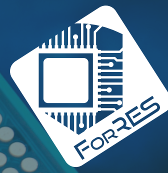


Factsheet 3: Delayering Techniques in Silicon Devices

Delayering is a process used in semiconductor analysis to sequentially remove layers from a silicon device to expose underlying structures for investigation. It is critical in failure analysis, reverse engineering, and research and development. The techniques involve precision mate-rial removal while maintaining the integrity of lower layers for examination. ForRES aims to im-prove delayering techniques to be suitable for modern semiconductor technology. This fact sheet aims to provide a concise overview of delayering techniques in silicon devices, covering its key features and how it can be used in forensic research.

Core Elements of Delayering Techniques

Delayering techniques involve precise methodologies tailored to the intricacies of silicon de-vices. These core elements ensure the process is effective, minimally invasive, and yields high-resolution insights into device architecture.

1. **Layer Removal:** Controlled processes are used to eliminate specific materials (e.g., sil-icon, oxides, metals) without damaging underlying layers.
2. **Precision:** Given the nanometer-scale features of modern devices, delayering tech-niques must ensure accuracy to preserve device integrity.
3. **Material-Specific Methods:** Techniques vary depending on the type of layer, such as conductive metals, insulating oxides, or semiconducting silicon.

Key Objectives

- **Failure Analysis:** Identify defects or weaknesses in the device.
- **Reverse Engineering:** Under-stand the design and fabrication process.
- **Debugging:** Isolate issues at dif-ferent layers of the silicon device.
- **Quality Control:** Ensuring consis-tency in manufacturing processes.

Key techniques in Delayering

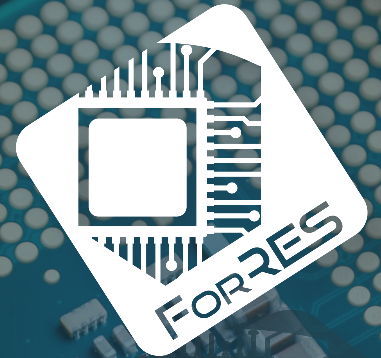
- **Mechanical Delayering:** Mechanical delayering involves the physical remov-al of mate-rial layers through abrasion or polishing. This is typically achieved by using tools like lapping machines, diamond-tipped abrasives, or abrasive grinding discs like silicon carbide and Alu-minun oxide. It is one of the simplest and most cost-effective methods for delaying, making it a popular choice for initial bulk material removal.
- **Chemical Delayering:** Chemical delayer-ing relies on the use of chemical etchants to selectively dissolve specific materials within a device. For example, acids or al-kalis can be used to target and remove layers like silicon dioxide, metals, or other compounds. This technique is highly ef-fective for selective material removal and minimizes mechan-ical stress on the sam-ple. However, it requires precise control over the etching time and concentration of chemicals to avoid unintended dam-age to adjacent layers.
- **Plasma Etching:** Plasma etching utilizes reactive plasma to remove material layers from the device. This process is typically carried out in a vacuum chamber using Reac-tive Ion Etching (RIE) equipment. Plasma etching is highly controlled and precise, allow-ing for nanoscale layer re-moval without direct physical contact. It is particularly useful for removing thin films and maintaining fine structural de-tails.
- **Broad Ion Milling:** Broad ion milling is a dry etch method similar to plasma etch-ing, but it utilizes a parallel beam of ions. The removal is achieved through a phys-ical sputtering process if inert gas like ar-gon is used. The etch selectivity between different materials can be finely tuned by adjusting the angle of incidence of the ion beam on the sample surface. It is also possible to employ a reactive gas for ion assisted etching. For more details please refer to Factsheet 2.
- **Focused Ion Beam (FIB) Milling:** Fo-cused Ion Beam (FIB) milling uses a finely focused beam of ions, commonly gallium ions, to selectively mill away material lay-ers. This technique offers exceptional pre-cision and is ideal for targeted delayering at micro-scopic scales, such as when an-alyzing specific regions of interest within a silicon de-vice. FIB is often used in con-junction with imaging tools like Scanning Electron Micros-copy (SEM) for real-time monitoring.
- **Laser Ablation:** Laser ablation involves the use of a high-power laser to vaporize mate-rial layer by layer. This non-contact method reduces the risk of mechanical damage to the device and is effective for quickly removing larger areas of material. It is particularly useful for devices with thick layers or when speed is a priority.

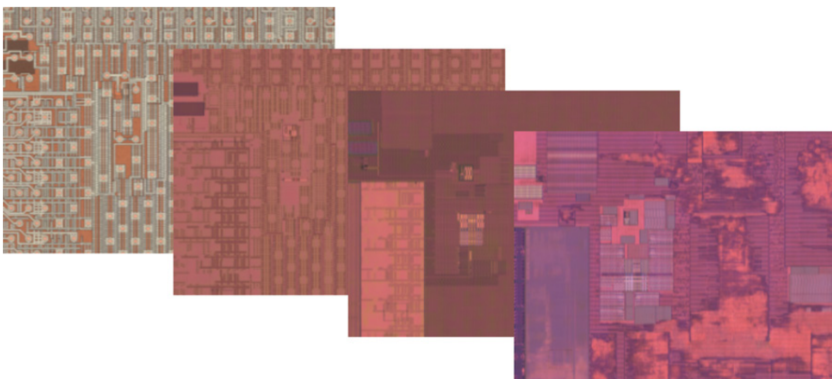
Applications for Forensic Research

Delayering techniques play a vital role in forensic research, particularly in cases involving counterfeit electronics, intellectual property theft, and hardware-based security investiga-tions. Here's how delayering is utilized in forensic contexts:

- **Counterfeit Detection:** Delayering is used to inspect the internal architecture of suspicious devices. By analyzing the internal layers and comparing them with known authentic designs, forensic experts can detect discrepancies, such as missing or substituted layers, altered design elements, or non-conformant materials.
- **Reverse Engineering and Intellectual Property Theft:** Delayering allows forensic experts to reverse engineer a device by examining its internal structure. By removing the layers and observing the transistor-level design, it is possible to reconstruct the underlying functionality of the chip, revealing whether proprietary or confidential technology has been illegally copied.
- **Hardware Security and Maleware Investigation:** Delayering can reveal hidden components such as malicious circuits or "hardware implants" designed to intercept or modify device behavior. By carefully examining each layer of the chip, forensic investigators can detect embedded threats that evade software detection.
- **Trace Evidence for Criminal Investigations:** Delayering is used in criminal investigations to uncover tampering or identify critical data traces left behind in electronic devices. For example, investigators may use delayering to retrieve hidden data storage or authentication keys embedded in the hardware.

Highly accurate delayering techniques are crucial in the field of semiconductor analysis, offer-ing a detailed view of the internal structures of silicon devices. In forensic research, it has broad applications, including the detection of counterfeit electronics, reverse engineering for intellectual property protection, hardware security investigations, and criminal evidence gathering. The precision and versatility of delayering techniques make them an indispensable tool for forensic experts and engineers alike in today's highly complex technological landscape.





Series of Images showing the first layers of a modern Finfet technology chip. For each layer sev-eral processing steps are required to achieve a planar surface ready for SEM imaging.

POLITIET
KRIPOS

Consortium
5 Partners
5 Countries

Budget
€ 2.3 Million
90% EU-funded

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24 Months
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